WE CLAIM:

1. A digital receiving device capable of separating simultaneous signals in a single channel, comprising:

digital signal receiving means;

means for performing a first fast Fourier transform on a digital signal;

means for performing a second fast Fourier transform on an output from said first fast Fourier transform;

a digital filter bank receiving output from said second fast Fourier transform;

a digital filter bank output clock cycle delaying means;

a digital filter bank output signal eliminating threshold; and

a plurality of narrow-band monobit receivers for receiving signals output from said digital filter bank and of a greater value than said signal eliminating threshold and further, said plurality of narrow-band receivers receiving only the highest two bits from real and imaginary parts of said signal output from said digital filter bank and of a greater value than said signal eliminating threshold.

2. The digital receiving device of claim 1 wherein a bandwidth of said plurality of narrow-band monobit receivers is wider than 93.75 MHz.

3. The digital receiving device of claim 1 wherein said digital receiving device can separate two signals separated by 12 MHz.

4. The digital receiving device of claim 1 wherein said monobit receivers receive 16 complex inputs and processing 16 outputs covering a bandwidth of 187.5 MHz with each individual output covering a bandwidth of 11.72 MHz.

5. The digital receiving device of claim 1 wherein said digital filter bank output cycle clock delaying means further comprises two delay lines between each filter output.

6. The digital receiving device of claim 1 wherein said digital filter output signal sampling rate is 187.5 MHz.

7. The digital receiving device of claim 1 wherein said monobit receivers have a bandwidth of 187.5 MHz.

8. The digital receiving device of claim 1 wherein said plurality of narrow-band monobit receivers comprises 16 narrow-band monobit receivers.

9. The digital receiving device of claim 1 further comprising a phase comparator after said plurality of monobit receivers for a finer frequency reading.

10. The digital receiving device of claim 1 wherein said means for performing a second fast Fourier transform on an output from said first fast Fourier transform comprises a monobit receiver.

11. A digital receiving device capable of separating two signals separated by 12 MHz comprising:

digital signal receiving means;

means for performing a first fast Fourier transform on a digital signal;

means for performing a second fast Fourier transform on an output from said first fast Fourier transform;

a digital filter bank receiving output from said second fast Fourier transform;

a digital filter bank output clock cycle delaying means comprising two delay lines between each filter output;

a digital filter bank output signal-eliminating threshold;

a plurality of narrow-band monobit receivers for receiving signals output from said digital filter bank and of a greater value than said signal eliminating threshold, said plurality of narrow-band receivers receiving only the highest two bits from real and imaginary parts of said signal output from said digital filter bank and of a greater value than said signal eliminating threshold and wherein said monobit receivers receive 16 complex inputs and processing 16 outputs covering a bandwidth of 187.5 MHz with each individual output covering a bandwidth of 11.72 MHz; and

a phase comparator receiving output from said plurality of monobit receivers for a finer frequency reading.

12. A digital signal receiving method capable of separating simultaneous signals in a single channel, comprising the steps of:

receiving a digital signal;

performing a first fast Fourier transform on said digital signal;

performing a second fast Fourier transform on an output from said first fast Fourier transform;

receiving output from said second fast Fourier transform into a digital filter bank;

delaying said digital filter bank output;

eliminating a digital filter bank output signal based on a preselected threshold; and

receiving signals output from said digital filter bank through a plurality of narrow-band monobit receivers of a greater value than said signal eliminating threshold, said plurality of narrow-band receivers receiving only the highest two bits from real and imaginary parts of said

signal output from said digital filter bank and of a greater value than said signal eliminating threshold.

13. The digital signal receiving method of claim 12 wherein said step of receiving signals output from said digital filter bank further comprises receiving signals output from said digital filter bank through a plurality of narrow-band monobit receivers having a bandwidth wider than 93.75 MHz.

14. The digital signal receiving method of claim 12 wherein said digital receiving method separates two signals separated by 12 MHz.

15. The digital signal receiving method of claim 12 wherein said step of receiving signals output from said digital filter bank through a plurality of narrow-band monobit receivers further comprises the step of receiving signals having 16 complex inputs and processing 16 outputs covering a bandwidth of 187.5 MHz, with each individual output covering a bandwidth of 11.72 MHz output from said digital filter bank through a plurality of narrow-band monobit receivers.

16. The digital signal receiving method of claim 12 wherein said delaying step further comprises the step of delaying said digital filter bank output cycle clock with two delay lines between each filter output.

17. The digital signal receiving method of claim 12 wherein said step of receiving signals output from said digital filter bank further comprises receiving signals output from said digital filter bank through 16 narrow-band monobit receivers.

18. The digital signal receiving method of claim 12 further comprising the step of comparing the phase of the output of said plurality of monobit receivers for a finer frequency reading.